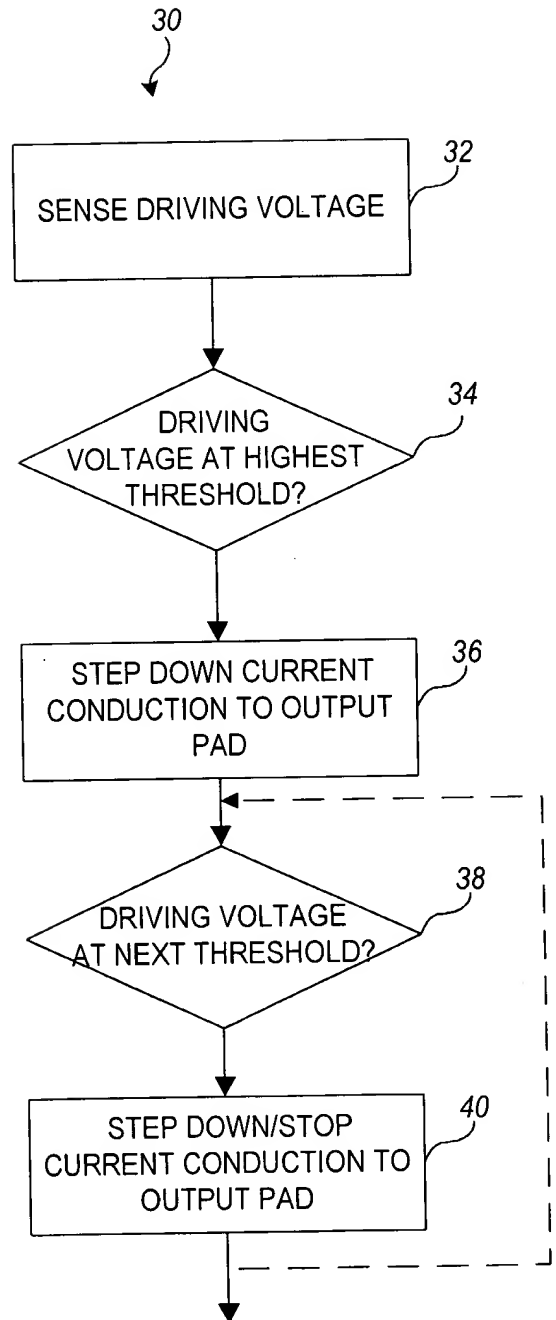
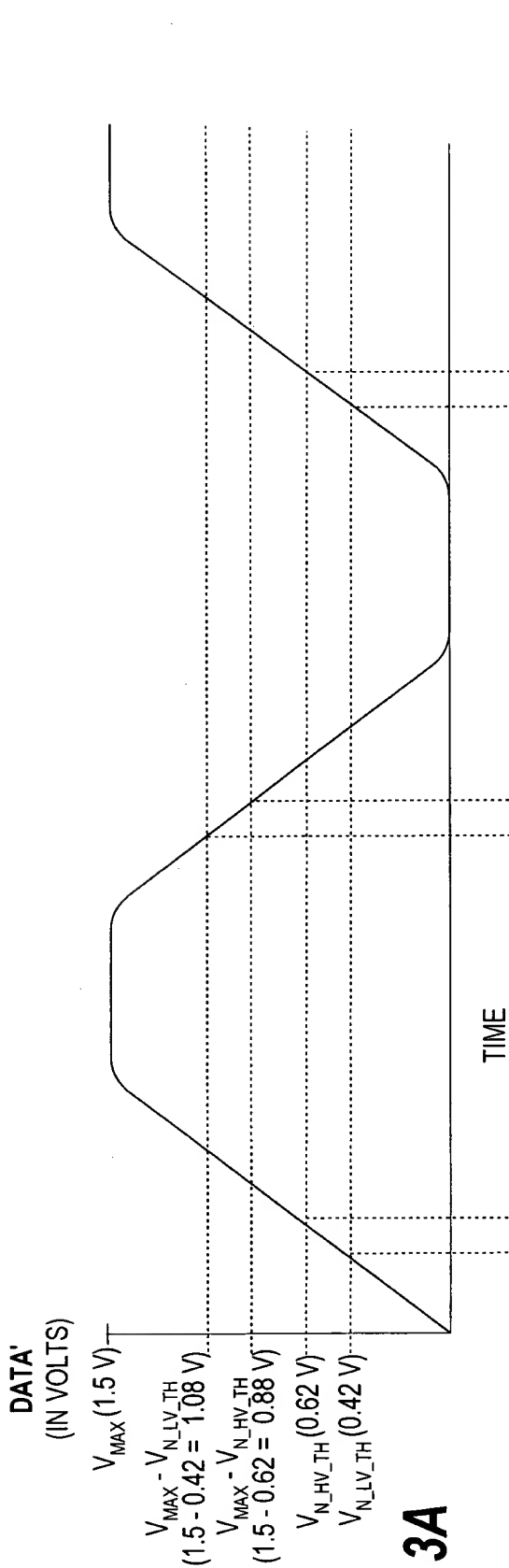


**FIG. 1A**

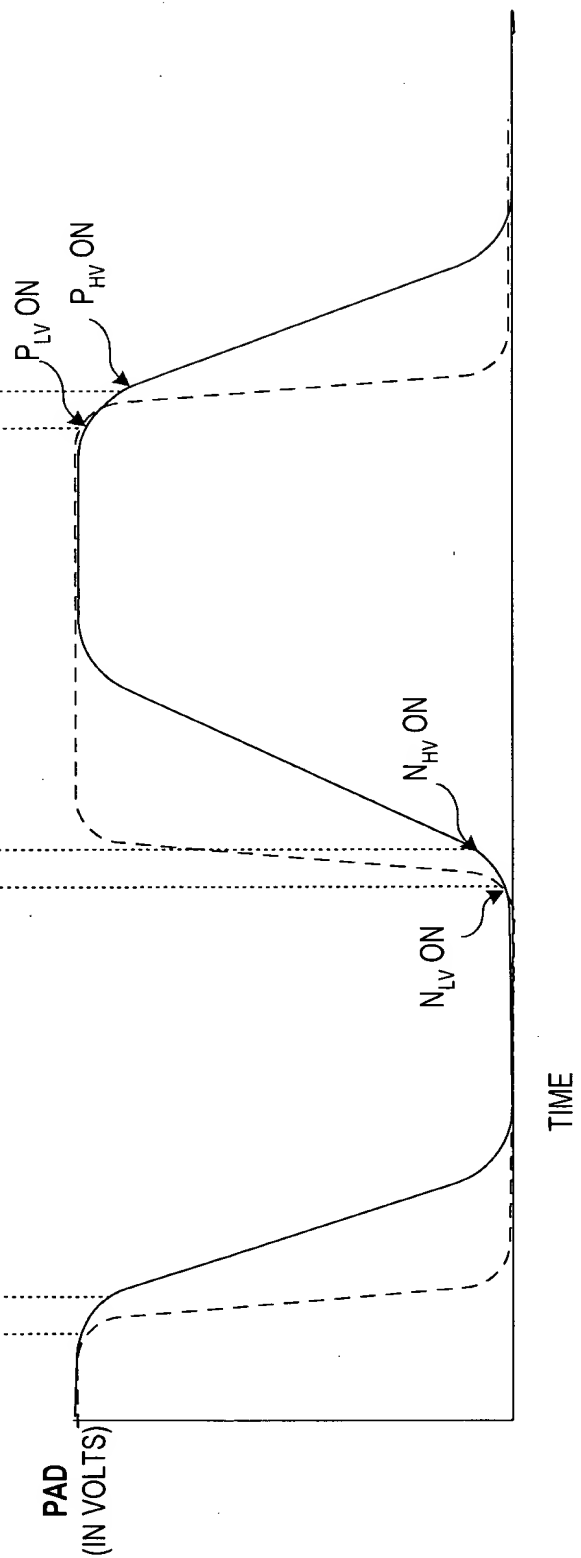


**FIG. 1B**

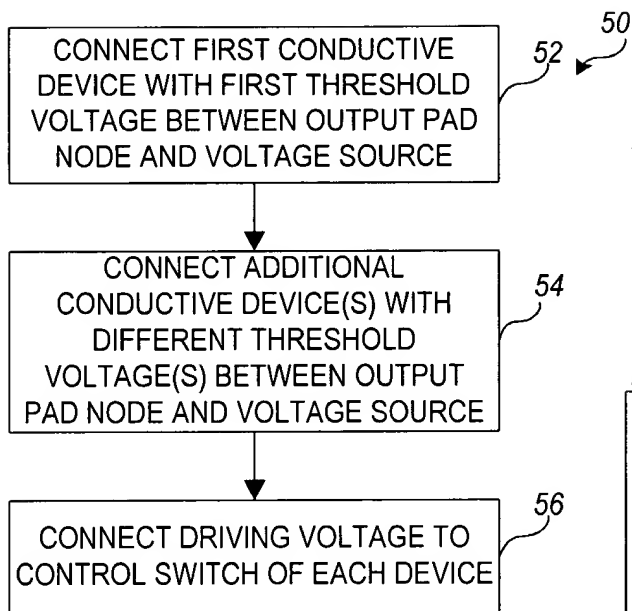
The circuit diagram (100) illustrates a multi-bit data bus system. It features two data inputs, S1 and S2, each represented by a bus of inverters (110, 120). The output of S1 is DATA', and the output of S2 is DATA'. These signals are connected to a series of PMOS transistors (112, 122) and NMOS transistors (114, 124) that form a multi-bit output bus (PAD). The PMOS transistors are labeled P<sub>LV</sub> and P<sub>HV</sub>, and the NMOS transistors are labeled N<sub>LV</sub> and N<sub>HV</sub>. The circuit is powered by V<sub>DD</sub> and ground. The output bus (PAD) is connected to a multi-bit output (150).



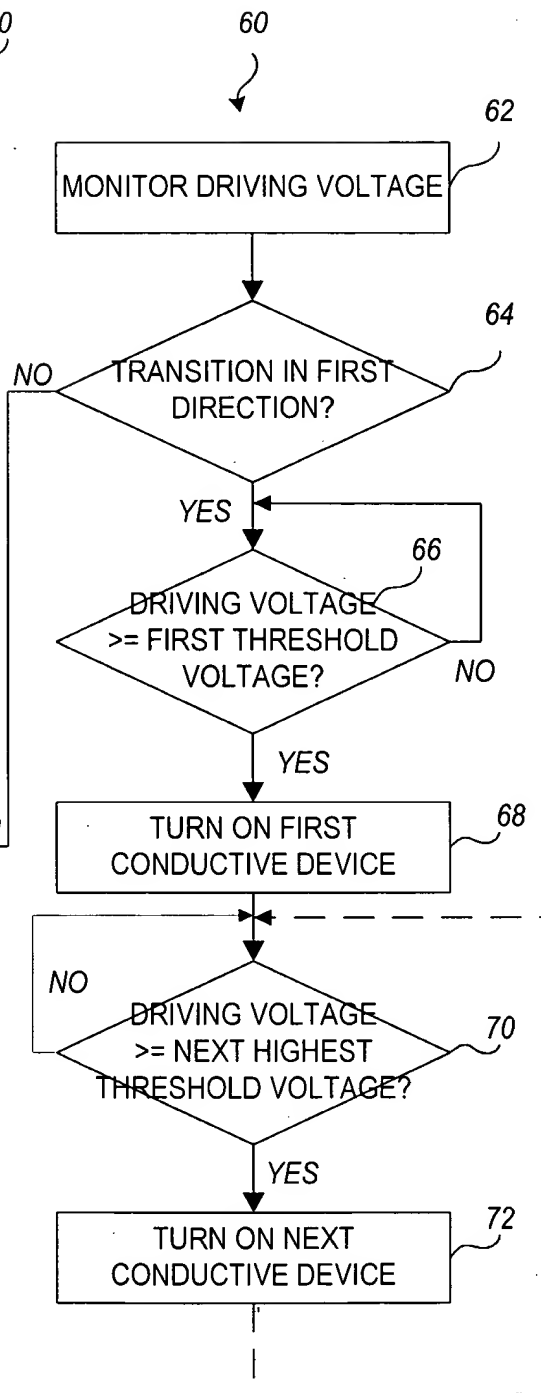
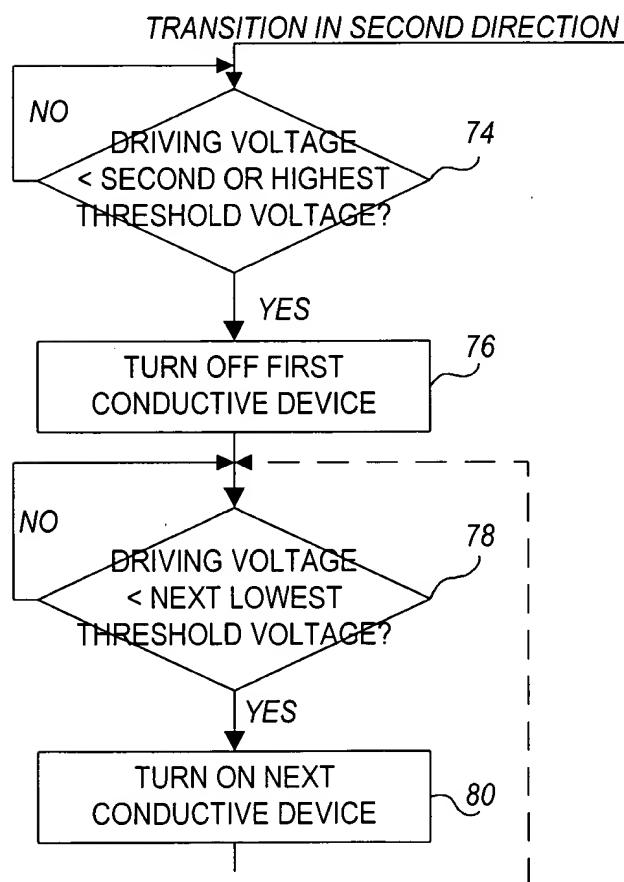
**FIG. 3A**



**FIG. 3B**



**FIG. 5**



**FIG. 6**